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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,996	04/03/2001	Tadaaki Yamauchi	57454-066	6448

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EXAMINER
SONG, JASMINE

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,996	YAMAUCHI ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 1-16 are represented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings filed on 04/03/2001 have been approved by the Examiner.

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Information Disclosure Statement

5. The information disclosure statement filed 04/03/2001 fails to comply with 37 CFR 1.98(a)(1), which requires a list of all patents, publications, or other information submitted for consideration by the Office. It has been placed in the application file, but the information referred to therein has not been considered.

6. The information disclosure statement (IDS) submitted on 12/31/2001 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Motomura., U.S. Patent 6,338,108 B1.

Regarding claim 1, Motomura teaches that a semiconductor memory device (Fig.8, the coprocessor-integrated packet-type DRAM 1), comprising:

a terminal group (Fig.8, External I/O terminal 5) receiving an externally applied control signal, address, and data (col.21, lines 14-16);

a memory cell array (Fig.8, the DRAM core section 15 within the memory section 11) transmitting/receiving said data (reading or writing operation) to/from a region (a desired DRAM bank 17) designated by said address (col.30, lines 29-33) in accordance

with said control signal (Fig.8, control signal register 20) (Fig.15 and 16, col. 30, lines 56 to col.31, lines 12); and

a logic circuit (Fig.8, control section 12) processing data in accordance with at least one of said control signal, address, and data (col.21, lines 14-16, control signal, an address which is designated in the parameter fields, data packet) when said address designates a prescribed first region (it is taught as the parameter field in the request packet designates a memory control register 29 as shown in Fig. 8, col.31, lines 17-20) if said control signal, address, and data are applied to said terminal group in a sequence of applying said control signal, address, and data to said memory cell array (col.31, lines 2-12 and lines 28-35).

Regarding claim 2, Motomura teaches further comprising an interface portion (Fig.8, element 13) receiving said control signal, said address, and said data from said terminal group for instructing an operation in accordance with at least one of said control signal, said address, and said data with respect to at least one of said memory cell array (as shown in Fig.8) and said logic circuit (Fig.8, control section) in accordance with said address, said logic circuit including

a data holding portion (control signal register, write data register and read data register as shown in Fig.8) for holding a content of the instruction (data packet) from said interface portion, and

a data processing circuit (Fig.8, coprocessor section 14) for processing data according to the content held in said data holding portion.

Regarding claim 3, Motomura teaches that said instruction content includes a command (Fig.13) for designating an operation of said data processing circuit (read or write operation of the coprocessor section 14), and input data (data read /write between the DRAM core section and write or read data registers) processed by said data processing circuit, and said holding portion includes

a first holding circuit holding said command (write or read data register include the data packet which having the command as shown in Fig.13 or Fig.17, subcommand),

a second holding circuit holding said input data (Fig.17, operation parameter writing), and

a third holding circuit holding a result of said data processing circuit resulting from said input data (Fig.17,operation result request).

Regarding claim 4, Motomura teaches that said data holding portion further includes a fourth holding circuit holding a flag indicating as to if the data process has been completed by said data processing circuit (Fig.17, operation status reading).

Regarding claim 5, Motomura teaches that said data processing circuit performs an encryption process is taught as the verification process of coprocessor (col.28, lines 63 to col.29, lines 12), and said input data includes key data of a cipher (it is taught as decoding the device ID).

Regarding claim 6, Motomura teaches that said instruction content (data packets) includes designation of a plurality of operation modes (Fig.17, writing access or reading access) of said data processing circuit, and

said data holding portion has a holding circuit (Fig.9C, request interface section 13-3) holding said plurality of operations modes, said holding circuit has a capacity of bits corresponding to data written to said memory array at a time (Fig.13F), and

the designation of said plurality of operation modes with respect to said logic circuit is performed in a sequence of one operation of writing data to said memory cell array (col.31, lines 2-12 and lines 28-35).

Regarding claim 7, Motomura teaches that said interface portion (Fig.8, element 13) includes a mode register (Fig.9B, request interface section 13-3) which can be rewritten in accordance with said control signal (col.22, lines 54-56), and

said interface portion determines a portion of an address space to which said first region is allocated (col.30, lines 30-32) in accordance with a value (the value represents the read or write) held in said mode register.

Regarding claim 8, Motomura teaches that said prescribed first region is a portion of a real address space of said memory cell array is taught as the memory control register 29 is a portion of memory section 11 as shown in Fig.8 and memory access to memory control register section 29 as the independent access operation.

Regarding claim 9, Motomura teaches that said prescribed first region is a portion of a virtual address space other than a real address space of said memory cell array is taught as the first region 29 can be used as storing the address from the coprocessor section 14 which is the virtual address to access the DRAM core section as shown in Fig.8.

Regarding claim 10, Motomura teaches that said logic circuit (Fig.8, control section 12) processes data stored in said address space of said memory cell array corresponding to said prescribed first region in accordance with access to said prescribed first region which is a portion of said virtual address space (as explained in the rejection of claim 9).

Regarding claim 11, Motomura teaches that method of controlling a semiconductor memory device (Fig.8, the coprocessor-integrated packet-type DRAM 1) including a terminal group (Fig.8, External I/O terminal 5) receiving an externally applied control signal, address, and data (col.21, lines 14-16), a memory cell array (Fig.8, the DRAM core section 15 within the memory section 11) transmitting/receiving said data (reading or writing operation) in accordance with said control signal (Fig.8, control signal register 20) to/from a region (a desired DRAM bank 17) designated by said Address (col.30, lines 29-33) (Fig.15 and 16, col. 30, lines 56 to col.31, lines 12), and a logic circuit (Fig.8, control section 12) processing data in accordance with at least one of said

control signal, said address, and said data (col.21, lines 14-16, control signal, an address which is designated in the parameter fields, data packet) when said address designates a prescribed first region (it is taught as the parameter field in the request packet designates a memory control register 29 as shown in Fig. 8, col.31, lines 17-20) if said control signal, said address, and said data are applied to said terminal group in a sequence of applying said control signal, said address and said data to said memory cell array (col.31, lines 2-12 and lines 28-35), said method comprising:

the step of designating said first region (it is taught as the parameter field in the request packet designates a memory control register 29 as shown in Fig. 8, col.31, lines 17-20) as a reserved region (it is taught as the memory access to memory control register section 16 in the memory section 11); and

the step of designating said first region by said address in a sequence of writing to said memory cell array (col.31, lines 2-12 and lines 28-35) and applying a command to said logic circuit (col.30, lines 29 to col.31, lines 26, as shown in Fig.13A-D, data packet includes commands).

Regarding claim 12, Motomura teaches further comprising the step of designating said first region (col.31, lines 2-12 and lines 28-35) in a sequence of reading from said memory cell array (col.31, lines 2-12 and lines 28-35) and reading a process result of said logic circuit (col.31, lines 31-33).

Regarding claim 13, Motomura teaches that said semiconductor memory device (Fig.9A, element 1) is connected to a microcomputer (microprocessor 9) internally provided with a cache memory (col.8, lines 66 to col.9, lines 5 and col.37, lines 39-45, further, it is well known in the art the microprocessor includes the cache memory) through said terminal group (Fig.9A element 5), and said method further comprises the step of designating said first region as a region not using said cache memory is taught as the memory control register 29 is reserved memory region for memory access to memory access between the control section and the memory control register section.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motomura., U.S. Patent 6,338,108 B1, in view of Maruyama et al., U.S. Patent 6535412 B1.

Regarding claim 14, Motomura teaches that a semiconductor memory device (Fig.8, the coprocessor-integrated packet-type DRAM 1), comprising:

a first terminal group (Fig.8, External I/O terminal 5) receiving an externally applied control signal, address, and data (col.21, lines 14-16);

a memory including a plurality of memory cells arranged in rows and columns (Fig.8, the DRAM core section 15 within the memory section 11) and transmitting/receiving said data (reading or writing operation) in accordance with said control signal (Fig.8, control signal register 20) with respect to a region (a desired DRAM bank 17) designated by said address (col.30, lines 29-33); and

a logic circuit (Fig.8, control section 12) for processing data in accordance with at least one of said address and data (col.21, lines 14-16, control signal, an address which is designated in the parameter fields, data packet).

Motomura does not teach that a memory and the logic circuit are activated in accordance with the select signal and activated in a complementary manner.

However, Maruyama teaches that a memory and the logic circuit are activated in accordance with the select signal and activated in a complementary manner (Fig.13, col.13, lines 60 to col.14, lines 12).

As taught by Maruyama, the use of selecting signal and activating function in a complementary manner is advantageous for ease of ~~to easy to~~ design and the accompanying circuit scale can be reduced (col.4, lines 17-20). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Maruyama in the system of Motomura and have the selecting signal and activating function in a complementary manner for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated

one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 15, Motomura teaches that said memory performs an operation of selecting said memory cell in accordance with said address including a row address and a column address time divisionally applied to said first terminal group (col.35, lines 62 to col.36, lines 8), and said logic circuit performs an operation in accordance with said address is collectively applied to said first terminal group (col.35, lines 32-42).

Regarding claim 16, Motomura teaches that said logic circuit includes an ATD circuit detecting changes in said row address and said column address for generating an operation timing (Fig.19 and 20, col.36, line 33 to col.37, lines 25).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Taito et al.,	US 6317368 B1
Ohtani et al.,	US 6130852
Fujimoto et al.,	US 6122214
Takase	US 6134174
Komoike	US 6367044 B1
Takase	US 6370080 B2

12. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7238 for regular communications and 703-746-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song
Patent Examiner
September 5, 2003

Mano Padmanabhan
Supervisory Patent Examiner
Technology Center 2100